Preliminary Specifications for the Analog & Digital Sections of the Forward Silicon Tracker Readout Chip (FSSR)

BTeV Document 3638

Revision 3

23 November 2004

Authors

Valerio Re, et. al.

Valerio Re
Università di Bergamo – INFN Pavia
Dalmine (BG), 24044, Italy
E-Mail: *valerio.re@unibg.it*
Phone: *(39) 035-2052311*
FAX: *(39) 035-562779*

Table of Contents

Document Revision History

Revision Number	Date	Description
1	2 November 2004	First draft of the FSSR Preliminary Specifications document (analog section).
2	10 November 2004	Specs for the internal pulser were added (besides minor corrections and additions).
3	23 November 2004	A description of the digital section was added.

1 Introduction

A major component of the BTeV detector is the Forward Silicon Tracker. It is made of 7 stations of silicon strip detector planes. Each station contains 3 planes arranged in an X, U, V orientation for a total of 129,000 silicon strip channels in the BTeV detector. Each channel requires readout electronics to measure the hit information from each strip. A full custom integrated circuit called the FSSR (Fermilab Silicon Strip Readout) chip has been designed in the TSMC 0.25 μm CMOS process to interface with the silicon strip detectors and send digital information to the data acquisition system.

This draft establishes the specifications of this custom-designed integrated circuit (IC) for the front-end processing of the signals from the silicon strip detectors in the BTeV Forward Tracker.

2 Functional Specifications

2.1 Analog Circuitry

The analog section of the IC consists of 128 channels, each connected to a detector strip. The signals from the strips, after amplification and shaping are compared to a preset threshold. To achieve the required position resolution, the channels provide a binary information (hit / no hit), generating a logic 1 at the output if a signal exceeding the threshold is detected. An additional 3 bit analog information is provided by a Flash ADC for calibration and monitoring purposes.

Figure 2.1-1 shows a schematic representation of the architecture of the analog section, which is described in the following.

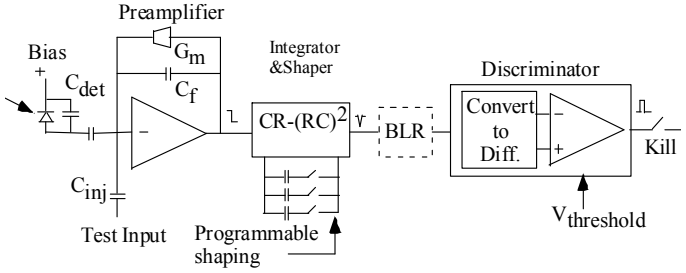

Figure 2.1-1. Analog section of the FSSR chip.

2.1.1 Analog Power Supply and Ground

Analog signal processing is combined with digital readout logic on a single CMOS chip. Therefore, isolation is provided between analog electronics and digital interferences. The analog section has its own power supply and ground which are separate from those used in the digital section.

- **Specification 2.2.1-1 (Analog Power Supply):** The analog section uses a single power supply (+2.5 V).
- **Specification 2.2.1-2 (Analog Power Dissipation):** The power dissipation of the analog section is ≤ 4 mW/channel.

2.1.2 Preamplifier

The first stage in the signal processing is a charge-sensitive preamplifier. It has a continuous reset, so that it is active at all times, including the time during which data are being digitized and read out. The preamplifier has a fast rise time, so that the overall bandwidth is determined by the shaper stage and, therefore, is not significantly influenced by the detector capacitance C_D. The noise specifications refer to the typical value of the detector capacitance and of the signal peaking time t_P. The charge sensitivity G_Q or gain is programmable. Two values can be chosen to increase the channel dynamic range (lower gain) or decrease the threshold dispersion (higher gain). The gain is adjusted by changing the value of the feedback capacitance C_f.

- **Specification 2.2.2-1 (Preamplifier Specifications):** The charge sensitive preamplifier has specifications as given in Table 2.2.2-1.

Table 2.2.2-1

Preamplifier Specifications

Charge sensitivity	Programmable, G_Q = 6.5 mV/fC (C_f = 150 fF) or 10 mV/fC (C_f = 100 fF)
Reset	Continuous
Rise time	t_r = 10 ns
Equivalent Noise Charge at C_D = 20 pF and t_P = 85 ns, 500 nA detector leakage current	ENC ≤ 1000 e rms

2.1.3 Pulse shaping

Signal shaping after the preamplifier is achieved by two stages, an integrator and an active filter (shaper) performing one more integration and a differentiation. The shaper is optimized to handle signals delivered from p-type strips as in the BTeV silicon tracker. The gain is boosted up to about 100 mV/fC or 150 mV/fC (the actual value depends on the programmed value of the preamplifier feedback capacitance, see subsection 2.2.2). The value of the peaking time is programmable by connecting different capacitors to the integrator and shaper. This allows operation with beam crossing times from 132 nsec to 396 nsec. A baseline restorer (BLR) can be included in the signal processing chain by acting on a programmable switch. The BLR cancels the baseline shifts due to the differentiation in the shaper stage, which may affect the threshold dispersion of the discriminator (see subsection 2.2.4). The BLR reduces the overall gain of the analog channel by about 20%.

- **Specification 2.2.3-1 (Pulse Shaping Specifications):** The pulse shaper has specifications as given in Table 2.2.3-1.

Table 2.2.3-1

Pulse Shaping Specifications

Shaping	$CR-(RC)^2$
Gain	≈ 15 (without BLR)
Peaking time	Programmable, t_P = 65 ns, 85 nsec, 105 nsec, 125 nsec
Baseline restoration	Programmable

2.1.4 Discrimination

A comparator is used to discriminate the amplified pulse. A threshold circuit converts the single-ended signal at the output of the shaping section to a differential signal. A differential dc threshold voltage is superimposed to the dynamic signal to drive the comparator. A differential threshold voltage is used to avoid possible crosstalk from the digital section. The threshold is adjustable by setting a single on-chip DAC. Individual noisy channels can be shut off between the discriminator and the input of the digital section.

- **Specification 2.2.4-1 (Discriminator Specifications):** The discriminator has specifications as given in Table 2.2.4-1.

Table 2.2.4-1

Discriminator Specifications

Threshold	Differential, set by on-chip DAC for all channels
Threshold dispersion	≤ 500 e rms
Channel mask (Kill)	The output of the discriminator can be disconnected by means of a programmable shift register

2.1.5 Analog-to-Digital Conversion

In the BTeV Forward Silicon Tracker, sufficient track resolution is achieved with 100 micrometer pitch silicon strip detectors and a binary readout in the FSSR. A low resolution (3 bit) Flash ADC is included in the FSSR chip to monitor detector performance with radiation. The signal at the output of the shaping section is applied to eight discriminators in parallel, one discriminator providing the binary information (see subsection 2.2.4) and seven discriminators used in the Flash ADC. Eight separate DACs are used to set the discriminator thresholds on the FSSR chip.

- **Specification 2.2.5-1 (ADC Specifications):** The ADC has specifications as given in Table 2.2.5-1.

Table 2.2.5-1

ADC Specifications

Resolution	3 bits
Dynamic Range	0 – 2 Minimum Ionizing Particles (MIPs)
Threshold	Differential, set by on-chip DAC for each discriminator in all channels
Threshold dispersion	≤ 500 e rms

2.1.6 Calibration and Test Circuitry

In the FSSR chip each channel has a capacitor through which charge may be injected into the input of the preamplifier for test and calibration purposes. A programmable register is used to mask the inputs such that the calibration signal only affects the selected channels. The calibration signal is generated on the chip, in response to a command. An on-chip 8-bit DAC is used to select the charge level of the pulse sent to the preamplifier.

- **Specification 2.2.6-1 (Calibration Pulser Specifications):** The calibration pulser has specifications as given in Table 2.2.6-1.

Table 2.2.6-1

Calibration Pulser Specifications

Injected Charge Range	$0 – Q_{max}$, $Q_{max} \geq 10$ fC (2.5 MIPs)
Calibration Resolution	≤ 0.08 fC
Calibration Pattern	A programmable register allows selection of an arbitrary pattern of channels into which charge is injected

2.2 Digital Circuitry & Timing

The FSSR chip can be considered as comprised of several parts as shown in Fig. 2.2-1. The first part is the core circuitry, which includes the 128 channels of analog electronics, sixteen sets of control logic (one set for every 8 input channels), and core logic, which communicates with the data interface and the rest of the core circuitry. The second part is the Programming Interface (PI) and associated registers and DACs. The PI accepts data and commands from a serial input bus and returns information upon request. Information from the PI is stored in programmable registers, which control DACs and program the chip. The third part is the Data Output Interface, which accepts data from the core, formats the data, and transmits it off the chip. Every time a strip is hit, the set number and channel number within the set is read out along with the BCO number, which is stored in the Core Logic.

The architecture of the FSSR digital back-end is based on the BTeV pixel readout chip, FPIX2. Many FPIX2 circuit blocks are used with either no modifications or only minor modifications. The I/O protocols for the two chips are identical.

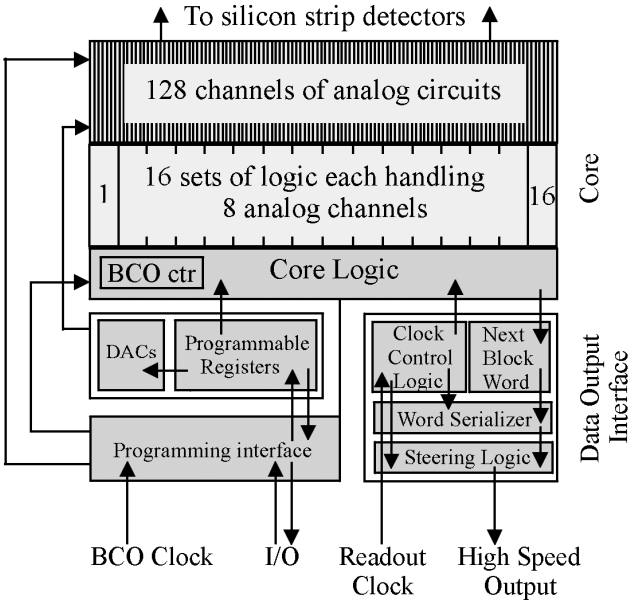

Figure 2.2-1. Block diagram of FSSR chip showing the core circuitry and the data output interface.

2.2.1 Core digital circuitry

As the other digital blocks, the architecture of the Core logic is based on the BTeV pixel readout chip, FPIX2. The 128 strips serviced by one chip are subdivided into 16 sets of 8 strips, as shown by Fig. 2.2-2, and each set is made to behave like a single column in the FPIX2 architecture. The ChipHit and ChipHasData lines shown in the picture are two diagnostic signals. In particular, ChipHit goes high whenever a discriminator fires while ChipHasData goes high every time the core has data to output. The readout is sparsified, that is, the Core transmits to the Data Output Interface only data relevant to channels where a hit is detected.

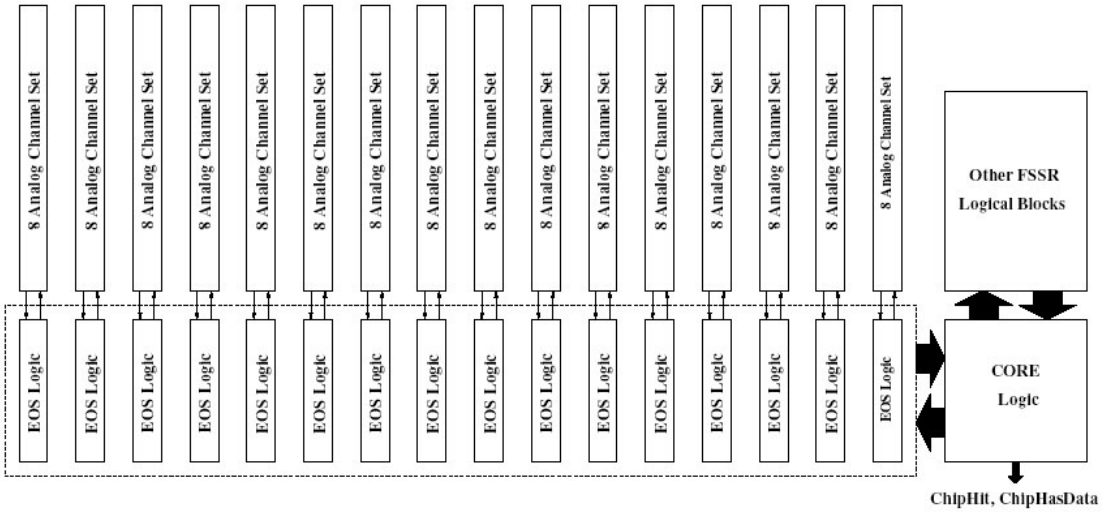

Figure 2.2-2 Block diagram of the FSSR core.

2.2.2 Programming Interface

The Programming Interface, Program Registers, and DACs are used to setup the chip and provide various control functions. Through the programming interface, all chips receive a serial string of bits, which includes 5 bits for chip ID, 5 bits for programmable register address, and 3 bits for instructions. Each chip has its chip ID set locally by means of 5 internal wire bonds. Information can be downloaded to one specific chip using the chip ID or all chips simultaneously using a wild chip ID address. There are 7 programmable registers:

CapSel is a 2 bit register used to set the desired shaping time in the analog section.

Kill is a 128 bit register used to disconnect the output of various discriminators in the analog section from the Core Logic.

Inject is a 128 bit register used to close a switch connecting various channels to an input pulse.

AqBCO (Acquire Beam Crossing) is an 8 bit register, which is used to hold the current value of the BCO counter in the FSSR. (The BCO counters in all FSSR chips are reset at the same time. Thus, system synchronization can be checked by loading the **AqBCO** register, reading it out later, and comparing results from all chips in the system.)

Alines is a 2 bit register used to set the number of serial output lines to 1, 2, 4 or 6.

SendData is a 1 bit register used to disable the core readout.

RejectHits is a 1 bit register used to inhibit the core from accepting any new hit information.

There are 3 other register addresses that are used for various types of resets but no information is stored.

The **CapSel**, **AqBCO**, **Alines**, **SendData**, and **RejectHits** registers have shadow registers and can be read out non-destructively at any time. The **Kill** and **Inject** registers do not have shadow registers. However, when they are read out, their contents are shifted back into the register input so that upon completion of read out, the data has been restored.

There are five instructions that can be executed for a given register address:

Write is used to download 2, 8, or 128 bits of information.

Read is used to read back information stored in a register.

Set is used to set all bits in a register = 1.

Reset is used to set all bits in a register = 0.

Default is used to set a register to its default value.

2.2.3 Data Output Interface

The FSSR has a data push type of readout architecture, which has been described elsewhere [2]. Data is output serially from the FSSR using LVDS. One feature of the Data Output Interface is the ability to program the number of serial output lines to be used depending on the expected hit activity in a given chip. A chip with low activity can use just one output serial pair while a chip in a very active area may have as many as 6 output pairs transmitting data off the chip. This means that no buffering of the output data is required on the chip. The Data Output Interface formats the information to be transmitted and adjusts the internal clocking frequencies so that all hit data in a single BCO is normally read out in about 1 BCO time interval.

The BCO clock may be either 3.78 MHz or 2.52 MHz. The FSSR readout clock is designed to be 70 MHz, and not tied to the BCO clock. Information is read out on both edges of the readout clock for a maximum data transmission rate of 840 Mb/sec. Status/Sync information and hit information are read out at different times depending on the hit activity in the chip. A readout word is comprised of 24 bits. The status/sync word has 10 bits of status, 13 bits for synchronization, and 1 bit for a word mark. The data word has 8 bits for the BCO number associated with the hit, 5 bits for the number of the logic set handling the hit, 4 bits for the number of the hit silicon strip, and 1 bit for a word mark (6 bits are currently unused). Data sent from the chip is not time ordered. The BCO number is used off line to reconstruct beam interactions. Since point-to-point communication is used, no chip ID information is needed in the data output.

The output data bit format changes when different numbers of output pairs are used. As mentioned, an output word is 24 bits long (b0 to b23). Fig. 6 shows how the bits are ordered for 1, 2, 4 or 6 output lines.

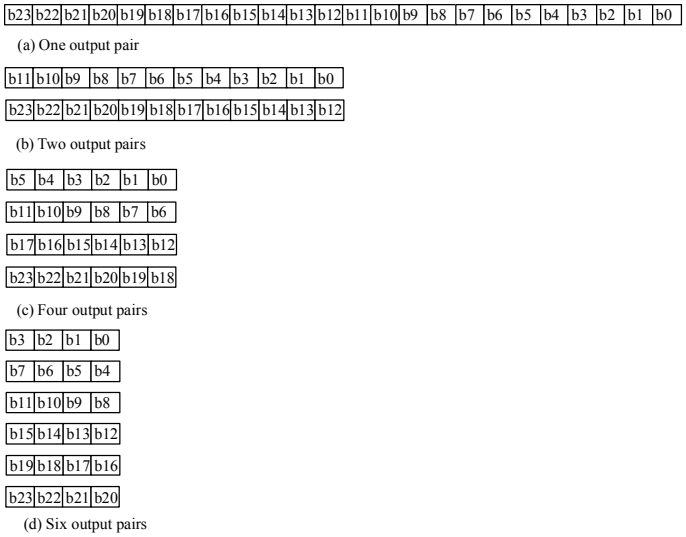

Fig. 2.2-2. Output data format with (a) one output pair, (b) two output pairs, (c) four output pairs, (d) six output pairs.

3 Operational Constraints

3.1 Radiation

Over the 10-year lifetime of the experiment, the FSSR chip is expected to see a total radiation dose of between 1 and 5 Mrad. To meet the radiation tolerance, the FSSR chip uses enclosed geometry transistors. Specially designed registers are used to mitigate SEU (Single Event Upset) effects.

3.2 Temperature

The FSSR ICs will be mounted on hybrid circuits that distribute power and signals, and thermally interface the ICs to the cooling system. The design of the cooling systems ensures that the temperature of the chips will not exceed + 40 °C.

4 Documentation

1. Valerio Re *et. al.*, "Status of the Design of the Analog Channel for the Strip Detector Readout (Feb. 2003)", BTeV-doc-1554-v2.
2. Valerio Re *et. al.*, "Status of the Design of the Analog Channel for the Strip Detector Readout (Dec. 2002)", BTeV-doc-1553-v2.
3. J. Hoff *et. al.,* "FSSR Status Report: Completion of the Functional Design Phase", BTeV-doc-1718-v4.
4. J. Hoff *et. al.,* "Readout Architectures for the BTeV Strip Detector", BTeV-doc-1551-v1.
5. L. Ratti *et. al.*, "The Fermilab Silicon Strip Readout Test Chip", BTeV-doc-2866-v1.
6. J. Hoff, A. Mekkaoui, D. Christian, S. Zimmerman, G. Cancelo, P. Kasper, R. Yarema, "PreFPIX2: Core Architecture and Results," *IEEE Trans. Nucl. Sci*, vol. 48, no. 3, pp. 485-492, June 2001.

▪